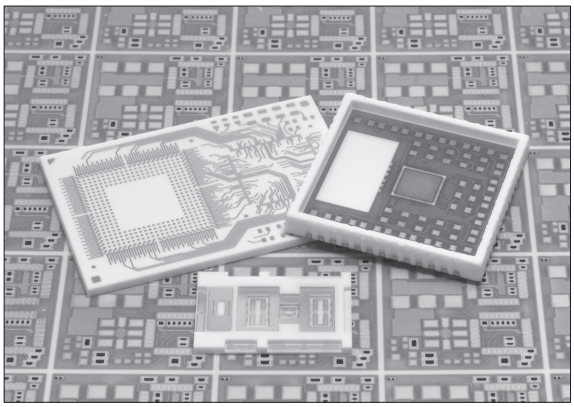
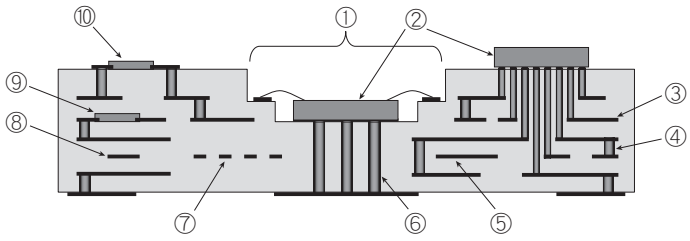
LOW TEMPERATURE CO-FIRED CERAMICS

EU RoHS

KLC LTCC低温共烧陶瓷多层基板
LTCC Multilayer Substrates



■ 结构图　Construction



①	空腔	Cavity	⑥	热通过	Thermal via
②	IC芯片	IC-chip	⑦	电感器	Inductor
③	导线分布图	Conductor pattern	⑧	传送线路	Transmission line
④	通过	Via	⑨	内层电阻	Buried resistor
⑤	电容器	Capacitor	⑩	表层电阻	Surface resistor

■ 特点　Features

- 是根据KOA公司独家的收缩控制技术和层叠技术的尺寸精度良好的多层基板。
- 由于精细的线路、模式，可以高密度布线。
- 可以通过L.C.带状传输线内层实现小型化。
- 由于低感电损失陶瓷和低损失导体，高频特性优良。
- 由于接近硅的热膨胀系数，是适于装配裸片的基板。
- 通过在裸片安装部设置热观测器，可提高放热性。
- 因为陶瓷的关系，耐热、耐湿性良好。
- 对应欧盟RoHS。
- Excellent size accuracy, byKOA's original shrinkage control technology and multi layer technology.
- The high-density wiring by the fine line and pattern is available.
- Miniaturization is possible by burying L, C and Strip-line.
- By the uses of low dielectric-loss ceramics and low loss conductors, the substrates excel in the high frequency characteristic.
- As the thermal expansion coefficient is close to silicon's, the substrates are suitable for the bare chip mounting.
- By preparing the thermal vias under bare chips, the substrates are excellent in the heat dissipation.
- The substrates are outstanding in heat resistance and humidity resistance due to the ceramics used.
- Products meet UE-RoHS requirements.

■ 收缩控制技术　Shrinkage Control Technology

LTCC在煅烧时会收缩，但通过精密控制材料、流程，实现了低于±0.05%的位置精度。
KOA公司的收缩控制技术有如下特点。
① 由于也能保持高度方向的精度，因而内层从动部件的特性，精度良好。
② 形成空腔时，可以形成稳定的空腔结构。

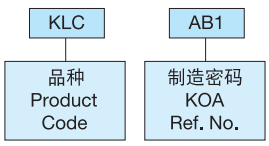
Although LTCC shrinks in the firing process, KOA has realized the position accuracy in ±0.05% or less by precisely controlling the process and the material.
There are the following features in the KOA shrinkage control technology:
① The accuracy of the height direction is maintained, so the characteristics and accuracies of buried passive components are outstanding.
② When a cavity is formed, the stable one can be formed.

■ 用途　Applications

- 使用微波、毫米波等的高频率的用途。
- 在高温、高湿度等环境严酷的环境下也可以使用。
- 移动体通信模块。
- 裸形片多芯片模块。
- MEMS包装。
- 转接基板
- UL1449(3rd Edition) (File No. E328032)
  NVD05, NVD07 : 82~470V, NVD10 : 82~1100V, NVD14 : 82~910V, NVD20 : 200~910V
- Applications using high frequencies like micro-waves, milli-waves, etc.
- Applications used in harsh environment, especially in high temperatures, high humidities, etc.
- Small size mobile communication modules.
- Multi chip modules for bare chips.
- MEMS packages
- Interposer substrates.

■ 品名构成　Type Designation

实例　Example



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■ LTCC是什么　What is LTCC

随着电子设备在高性能、轻薄短小方面的进展，在布线基板上也要求高性能。
作为对应基板高性能的技术之一，是LTCC（低温同步煅烧陶瓷）。
LTCC通过在氧化铝中加玻璃系材质，相比氧化铝在1500℃煅烧，可以在900℃以下的“低温”煅烧的陶瓷多层技术。
最大的特色是，通过低温煅烧，可以把银等低熔点材料在内部布线中使用。

With the high functioning and the advance in down-sizing of electronic equipment,wiring substrates are also required to be highly functioned.
One of the technologies to respond to the high functioning of the substrates is LTCC(Low Temperature Co-fired Ceramics), which is the ceramic multilayer technology that enables the alumina to be fired at a“low temperature”of 900℃or lower by adding glass materials to the alumina while it is fired by a“high temperature”of about 1500℃.
It is the LTCC’s important characteristics that low melting point materials like Ag, etc.can be used for the buried conductors for the low temperature firing.

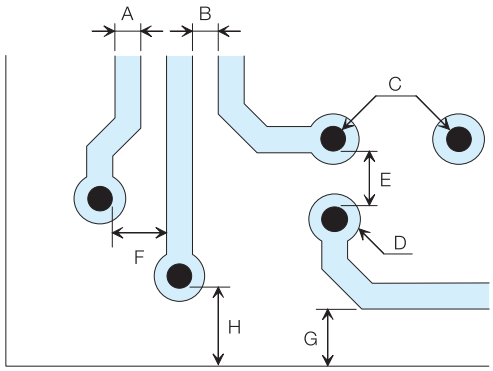
■ 基板材料特性　Characteristics of Substrate Material

项目 Parameter	特性 Characteristics
抗析强度（MPa） Bending strength	250
热膨胀系数（×10^{-6}/K） Thermal expansion coefficient	5.5
热传导率（W/m•K） Thermal conductivity	3
绝缘电阻（Ω•cm） Insulation resistance	＞10^{13}
介电常数 at 1MHz Dielectric constant	7
介质损耗 at 1MHz Dielectric loss	＜0.003
内部导体电阻（μΩ•cm） Resistivity of buried conductor	Ag 2.5
密度（g/cm^3） Density	2.8
表面光洁度 Ra（μm） Surface roughness Ra	＜0.4
耐压（kV/mm） Withstanding voltage	＞15
层厚（μm/Layer） Layer thickness	80, 100, 125 STD.

■ 设计规则　Design rule

符号 Symbol	项目 Parameter	设计值 Design value
A	线路宽度 Line width	0.06mm Min.
B	线路间空间 Line to line spacing	0.06mm Min.
C	通路直径 Via diameter	0.1mm, 0.15mm, 0.2mm
D	通路充填直径 Via pad diameter	Via diameter＋0.05mm Min.
E	通路间隔 Via to via spacing	0.2mm Min.
F	通路－线路间隔 Via to line spacing	0.15mm Min.
G	模型层通路充填直径 Part edge to conductor spacing	0.2mm Min.
H	基板端模型间隔 Part edge to Via spacing	0.3mm Min.
J1，J2	空腔宽度 Cavity width	0.6mm Min.
K1，K2	空腔深度 Cavity depth	0.1mm Min.
L	空腔壁面厚度 Wall thickness of cavity	0.5mm Min.
M	空腔内隔板宽度 Shelf width in the cavity	0.5mm Min.

表层・内层　Surface layer・Inner layer



空腔　Cavity